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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,200	04/21/2004	Cheng-Yuan Wu	VIAP0098USA	3199

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EXAMINER	
WATSON, CHARLES A	

ART UNIT	PAPER NUMBER
4117	

NOTIFICATION DATE	DELIVERY MODE
11/02/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/709,200	WU ET AL.	
	Examiner	Art Unit	
	Charles A. Watson	4117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claim 1 recites the limitation/clause "storing at least one packet transmitted to the network" in the context of the claimed invention seems inadequate. In accordance with the invention as set forth in the specification (e.g. par 0006), the packet processed stored in the memory seem to be the packets to be transmitted, rather than the packets received from the network which have already been transmitted. For examination purposes, the term will treated as the packet is going *to be* transmitted to the network, as per specifications, paragraph 0006. Thus, the claimed clause when interpreted insight of the specification, which as best understood should read the packet is *to be* transmitted.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1, 3 - 5,** and **7 – 9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Starr et al. (US 2004/0064590 A1) hereinafter referenced as Starr, in view of Lo et al. (US 6,667,983) hereinafter referenced as Lo.

Regarding **claim 1**, Starr discloses a network interface circuit (22) including a memory (42) for storing at least one packet *to be* transmitted to the network as shown on Fig. 1;

storing a packet data (e.g. file blocks) corresponding to a packet in the memory (paragraph 0063), and

transmitting the packet data to other sections (e.g. protocol stack) of the network interface circuit for processing the packet data (paragraph 0050 & Fig. 3);

However, Starr does not teach storing another packet data, which corresponds to another packet in the memory.

Lo teaches storing another packet data corresponding to another packet in the memory, a FIFO memory storing more than one packet pointer (col. 6, line 54-57).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made given the teachings of Starr and Lo. One would be motivated to combine these teachings because Lo teaches that the processor stores the new data packet into the register in the last vacant cell of the FIFO memory.

Regarding **claim 3**, Lo teaches where a portion of the packet data is process by other sections of the network interface circuit before the memory starts to store at least

a portion of another packet data for replacing the portion of the packet data (col 6, line 54-57).

Regarding **claim 4**, Lo teaches that the operation of the memory is first-in-first-out (col. 6, line 27-29).

Regarding **claim 5**, Lo teaches that the packet data is divided into a first portion and a second portion, when the first portion is transmitted to the network and the second portion is not transmitted to the network (col. 6; line 26-40). He also teaches that the memory starts to store at least a portion of another packet data (col. 6, line 54-57).

Regarding **claim 7**, Lo teaching the memory sequentially stores another packet data for replacing the first portion of the packet data (fig.1A & 2, col. 6, line 54-57).

Regarding **claim 8**, Starr teaches the network interface circuit is electrically connected to the memory (paragraph 0046),

a medium control module (52) of the network for processing a plurality of data stored in the memory (Fig.1 & paragraph 0058),

transmitting the processed data to the network (paragraph 0056 & fig. 2), the packet data originally stored in the memory is completely processed by the medium control module (paragraph 0058);

the memory starts to store another packet for replacing the packet data (Lo: col. 6; line 54-57).

Regarding **claim 9**, Lo teaches that a portion of the packet data processed by the medium control module is transmitted to the network; the memory starts to store another packet for replacing the portion of the packet transmitted to the network (col. 6; line 51-57).

4. **Claims 2 and 10 - 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Starr, in view of Lo, in further view of Hsu et al. (US 2003/0227928), hereinafter referenced as Hsu.

Regarding **claim 2**, Starr and Lo do not teach that the packet is completely processed by the other sections of the network interface card before the packet data is stored in the memory temporarily.

Hsu teaches that the packet data is completely processed by the other sections of the network interface card before the packet data is temporarily stored in the memory (paragraph 0037 & Fig.2).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made given the teachings of Starr and Lo. One would be motivated to combine those teachings with the teachings of Hsu because Hsu teaches that the MAC and the feature value evaluator prior being sent to the memory or buffer process data.

Regarding **claim 10**, Starr and Lo do not teach that the medium control module further includes a buffer, and data of the memory must first be stored in the buffer.

Hsu teaches that the medium control module further includes a buffer, and data of the memory must first be stored in the buffer (paragraph 0035 & fig. 2).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made given the teachings of Starr and Lo. One would be motivated to combine those teachings with the teachings of Hsu because Hsu teaches that operating system transfers the data packet, which is received by the MAC and stored in the buffer.

Regarding **claim 11**, Starr and Lo do not teach that the buffer is first-in-first-out.

Hsu teaches that the operation of the buffer is first-in-first-out (paragraph 0039).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made given the teachings of Starr and Lo. One would be motivated to combine those teachings with the teachings of Hsu because Hsu teaches that the data packet and the associated

Regarding **claim 12**, Lo teaches the memory starts to store another packet for replacing the packet data (col. 6; line 54-57).

Starr and Lo do not teach that original data stored in the memory is completely transmitted to the buffer.

Hsu teaches that the packet data originally stored in the memory is completely transmitted to the buffer (paragraph 0035).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made given the teachings of Starr and Lo. One would be motivated to combine those teachings with the teachings of Hsu because Hsu teaches that the data packets will be buffered in the memory. The occupied memory will not be released until the whole data file as been received to the buffer.

5. **Claim 6** is rejected under 35 U.S.C. 103(a) as being unpatentable over Starr, Lo, in view of Hsu, and in further view of Rajamony et al. (US 7,089,282), hereinafter referenced as Rajamony.

Regarding **claim 6**, Starr, Lo, nor Hsu manage to teach that the first portion of a data packet is overwritten by another packet data.

Rajamony teaches that the first portion of the packet data is overwritten by another packet data (col. 2; line 64-66).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made given the teachings of Starr, Lo and Hsu. One would be motivated to combine those teachings with the teaching of Rajamony because Rajamony teaches that NIC memory can act like a scratch buffer wherein it is constantly overwriting itself with packets that are about to be transmitted.

6. **Claims 13 - 16, 18 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Starr in view of Hsu.

Regarding **claim 13**, Starr teaches a network interface circuit for controlling data access of a network (paragraph 0053 & fig.1),

a medium control module for transmitting a packet to the network (paragraph 0046),

a memory for temporarily storing a packet data corresponding circuit to the packet (paragraph 0046)

Hsu teaches that the memory including a check circuit (value evaluator) (paragraph 0032);

wherein after the memory transmits the packet data to the medium control module the check circuit enables the signal (Hsu 0032 and 0046);

a memory access circuit (Hsu 0032);

wherein after receiving the interrupt request signal, the memory access circuit stores another packet data corresponding to another packet in the memory (Hsu 0046).

Regarding **claim 14**, Hsu teaches after the packet data is completely processed by the other sections of the network interface circuit (paragraph 0037 & Fig. 2). He also teaches that the check circuit sends the interrupt request signal (paragraph 0035).

Regarding **claim 15**, Hsu teaches that the check circuit sends the interrupt request signal (paragraph 0035). Star teaches that a portion of the packet is processed by the other sections of the network interface circuit (paragraph 0056 & fig.1).

Regarding **claim 16**, Hsu teaches the medium control module further comprises a buffer; wherein before the medium control module completely transmits the packet data of the memory to the network, the buffer stores the portion of the packet data untransmitted to the network (paragraph 0037).

Regarding **claim 18**, Hsu teaches the operation of the buffer is first-in-first-out (paragraph 0039).

Regarding **claim 20**, Hsu teaches that the memory controls all other memory units (111) under a recycling memory unit (nonvolatile memory) operation (paragraph 0032 & fig. 1).

7. **Claims 17 and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Starr in view of Hsu, in further view of Lo.

Regarding **claim 17**, Starr and Hsu do not teach that memory is the FIFO memory.

Lo teaches the operation of the memory is first-in-first-out (col. 6; line 13 -16).

It would have been obvious to one of ordinary skill in the art at the time of the invention was given the teachings of Starr and Hsu. One would be motivated to combine those teachings with the teachings of Lo because Lo teaches that the FIFO memory contains memory cells which work in conjunction with each other.

Regarding **claim 19**, Starr and Hsu do not teach that the network interface circuit is a full duplex network interface circuit.

However, Lo teaches that the network interface circuit is a full duplex network interface circuit (fig.5 & col.7; line 64-66).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made given the teachings of Starr and Hsu. One would be motivated to combine those teachings with the teachings of Lo because Lo teaches in full duplex, the NIC can send and receive data packets at the same time with respect to network.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A. Watson whose telephone number is (571)270-3633. The examiner can normally be reached on Mon-Thurs 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Beatriz Prieto can be reached on 571-272-3902. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

C.W.
Patent Examiner

/Prieto B./
Supervisory Patent Examiner, Art Unit 4117